# CONTROLLING THE SET UP OF A MEMORY ADDRESS

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ABSTRACT OF THE DISCLOSURE

A circuit is provided for controlling the set up of a memory address. The circuit includes a first latch circuit for latching a first memory address in response to a first simultaneous occurrence of a predetermined value for an output enable signal and a predetermined value for a row address strobe signal. A second latch circuit is coupled to the first latch circuit. The second latch circuit receives the first memory address from the first latch circuit and latches the first row address thereafter for decoding. The first latch circuit can latch a second memory address in response to a second simultaneous occurrence of the predetermined value for the output enable signal and the predetermined value for the row address strobe signal, the second simultaneous occurrence occurring while the first row address is being decoded.